**SoC compatible 1T1C FeRAM memory array based on ferroelectric Hf0.5Zr0.5O2**

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**ABSTRACT**  **1T1C ARRAY INTEGRATION**   
 This paper experimentally demonstrates fundamental Fig.5 shows a cross section SEM image of the 64 kbit 1T1C memory array operation of a ferroelectric HfO2-based 1T1C FeRAM array. A MFM capacitor consisting of a FeRAM. Metal/ferroelectric/metal (MFM) capacitors TiN/HZO/TiN stack was successfully integrated directly on

consisting of a TiN/Hf0.5Zr0.5O2(HZO)/TiN stack were optimized for a sub 500 °C process. Structures revealed excellent performance such as remanent polarization 2Pr > 40 µC/cm2, endurance > 1011 cycles, and 10 years data retention at 85 °C. Furthermore, the MFM capacitors were successfully integrated into a 64 kbit 1T1C FeRAM array including our dedicated circuit for array operation. Back-end-of-line (BEOL) wiring showed no degradation of the underlying CMOS logic. Program and read operation were properly controlled resulting in 100 % bit functionality at an operation voltage of 2.5 V and operating speed at14 ns. This technology matches requirements of last level cash (LLC) and embedded non-volatile-memory (NVM) in low power System-on-a-Chip (SoC) for IoT applications.

**Keywords:** hafnium oxide, zirconium oxide, capacitor **INTRODUCTION**   
 Recently, ferroelectric HfO2-based FeRAM has been getting a lot of attention due to its high performance operation and CMOS compatible process [1-2]. Compared to ferroelectric FET (FeFET), 1T1C FeRAM has the advantage of higher endurance, lower voltage operation and disturb free operation [3]. However, a memory array operation using a dedicated circuit such as address decoders and a sense amplifier (SA) for the HfO2-based 1T1C FeRAM has never been reported. In this work for the first time, we fabricated a 64 kbit array using a ferroelectric HfO2-based 1T1C test chip with CMOS logic circuit and demonstrated good array operation yield. Furthermore, MFM capacitor size and operation condition dependency of the test chip on the read voltage margin supports the scalability of the SoC compatible LLC appreciations.

**MFM CHARACTERISTICS**   
 Intrinsic ferroelectricity of MFM capacitors was electrically confirmed on single large capacitors (Ø100µm). MFMs were fabricated including symmetrical TiN electrodes and 11 nm

top of the transistor allowing the crystallization anneal at 500°C prior to BEOL metal line processing. The capacitor process flow is shown in Fig. 6. A patterned bottom electrode (BE) is covered with HZO and the top electrode (TE). Fig.7 shows an optical microscope image of the 64 kbit test chip for ferroelectric HfO2-based 1T1C FeRAM. A dedicated circuit for 1T1C FeRAM operation with different size of capacitors ranging from 0.4 to 1.0 µm2 is integrated into the same chip.

**64 KBIT 1T1C ARRAY DEMONSTRATION**   
Fig.8 shows the read operation scheme of the 1T1C cell. A voltage change of VBL resulting from the transient capacitance difference (C0 vs. C1) of the two memory states of the ferroelectric capacitor (CFE) in comparison to a reference capacitor (CREF) is analyzed by an integrated SA using a step pulse sensing approach [5]. Simulation and experimental results of the detected VBL shown in Fig.9 reveals that this device is ideally functioning to separate both memory states (data0 and data1). Fig.10 shows the distribution of VBL obtained from both memory states for the 1T1C 64 kbit array based cells with a 1.0 µm2 capacitor size. A 100% bit functionalitywith a read voltage margin > 0.48V at 4 sigma tail is detected demonstrating a large signal margin even for arrays having a significantly higher density. Fig. 11 indicates a shmoo plot for an operating time from 1 ns to 50 ns and an operation voltage from 2.5 V to 3.5 V for both read and write operations of the test chip. No fail bit is observed for a 14 ns write and a 8 ns sense operation at 2.5 V each. Fig.12 shows the dependency of the read voltage margin on the MFM capacitors size. Dashed lines were calculated from the formula described in Fig.8(b). The obtained read voltage margin was in good agreement with the estimation for a 130 nm technology. As a result, a read voltage margin > 0.10V can be achieved using a <0.05 µm2 capacitor size which can be fabricated using a 40nm technology based 3D cylinder capacitor[7].

thick HZO deposited by ALD with 1:1 Hf:Zr ratio. Both 10 nm **CONCLUSION**

thick TiN electrodes were sputtered by PVD. The appearance of a ferroelectric orthorhombic phase was verified by grazing incidence X-ray diffraction (GIXRD) after a 500 °C crystallization anneal (Fig.1). A remanent polarization of 2Pr > 40µC/cm2 was achieved as indicated in the PE plot (Fig.2). Fig. 3 shows the endurance performance up to 109 cycles at 100 kHz cycling frequency. Negligible small changes of polarization were obtained during the data retention test at 85 °C for 100 min (Fig.4). These results suggest excellent performance with high reliability for integrated 1T1C FeRAM.

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We demonstrate a ferroelectric HfO2-based 1T1C FeRAM memory array suitable for system on chip (SoC) applications. MFM capacitors are successfully integrated into a 64 kbit array without any degradation of the underlying CMOS logic characteristics. For the first time, perfect yield and excellent operation performance for low voltages of 2.5 V at 14 ns operating speed was observed during array operation. This technology meets the performance of LLC and any other IoT applications of existing embedded memories as shown in table.1 in comparison to other technology options.

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|  | | | | | | | | | | | | | | Fig. 4: Data retention up to |
| Fig. 1: GIXRD spectrum of | | | | | Fig. 2: Polarization vs field | | | | Fig. 3: Cycling endurance at 100 | | | | |
| TiN/HZO/TiN stack after | | | | | hysteresis of a MFM capacitor | | | | kHz | (bottom | scale) | and | | 100 min baking time at 85 °C |
| 500 °C anneal | | | | with applied fields of 2.5-3.0 | | | | | projected endurance at 10 MHz | | | | | and projection to 10 years |
| MV/cm. | | | | | | | | (top scale) assuming same time | | | | | | with Same State(SS) [4]. |
| to break down. | | | | | | | | | | | | | | |
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| Fig. | 5: | Schematic | cross | Fig. 6: Process flow | | Fig. 7:Optical microscope | | | | | Fig. 8: Design of read out operation. (a) schematic | | | |
| section SEM image of MFM | | | | to fabricate MFM | | image of the 64 kbit 1T1C | | | | | of SA. 1T1C cell is connected to the bit line (BL), | | | |
| capacitors integrated within a | | | | below 500 °C BEOL | | FeRAM test chip. | | | | | word line (WL), and plate line (PL). (b) A formula | | | |
| BEOL process. | | | | budget. | | to determine the bitline voltage VBL (c) Definition | | | |
| of CFE in (b). | | | |
|  | | | | | | |  | | | | | | | |
| Fig. 9: (a) Timing diagram of a read operation as shown in Fig.8. | | | | | | | | Fig. 10: VBL distribution of the | | | | | Fig. 11: Shmoo plot of (a)write and | |
| VBL is precharged to 0 V during Δt0. VBL is sensed and compared | | | | | | | | 1T1C FeRAM for 64kbit at 2.5 | | | | | (b)sense time ranging from 1 ns to | |
| with reference voltage VREF during Δt1. If the VBL is larger than | | | | | | | | V with 100 ns operation at 1.0 | | | | | 50 ns and operation voltage ranging | |
| Vref, it is activated to VDD by sense enable pulse (SE) during Δt2 | | | | | | | | µm2capacitor size of the test | | | | | from 2.5 V to 3.5 V on the test chip. | |
| turning the state of CFE from data1 to data0. The data is written | | | | | | | | (Green: Pass, Red: Fail) | |
| chip. | | | | |
| back to data1 during Δt3. (b)Wave forms of the read operation | | | | | | | |

for data0 and data1 obtained by experiment for the test chip.

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|  | Table.1: Device structure comparison | **REFERENCE** |
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| Fig. 12: Read margin of the test chip 2.5 V 100 ns |
| operation as a function of capacitor size. Values of |

CBL were determined as 250 fF for the 130nm   
technology and 120 fF for 40nm technology [6].